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Electrical Characteristics Modeling of the Submicron MOSFETs Fabricated by Ultra-Thin-Silicon-on-Sapphire (UTSI SOS) CMOS Technology

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Abstract

Ultra-Thin-Silicon-on-Sapphire (UTSi SOS) is a perspective industrially exploitered CMOS technology for fabrication of novel highly integrated low power multimedia and wireless communication RF ICs. In this paper the TCAD and SPICE models of UTSi SOS MOFETs considering the characteristic features of UTSi SOS device structure were discussed. To verify the TCAD model, the fitting procedure for the parameters of trapped charge and mobility of electrons and holes in the Ultra-Thin channel layer was proposed. The version of compact SPICE UT SOI model for SOI/SOS MOSFETs considering the super-wide temperature range (-260°C…+300°C) was developed. The special sub-circuit was proposed to account for the kink effect.

Keywords: UTSI, SOS, TCAD, SPICE

Introduction

For many digital and analog VLSI circuit application low power dissipation and high speed are the most important parameters. So, the Ultra-Thin-Body (UTB) SOI MOSFET technologies fulfill the International Technology Roadmap for Semiconductors (ITRS) requirements for CMOS device downscaling [1].

Today the variety of two UTB Silicon-on-Insulator MOSFET devices are industrially exploitered to allow excellent channel control for high digital and analog performances: UTBB SOI (Ultra-Thin-Body-and-BOX on Silicon dioxide (SiO2) Insulator (see Figure 1, a) and UTSi SOS (Ultra-Thin-Silicon body on Sapphire (Al2O3) Insulator (see Figure 1, b)) [2, 3].

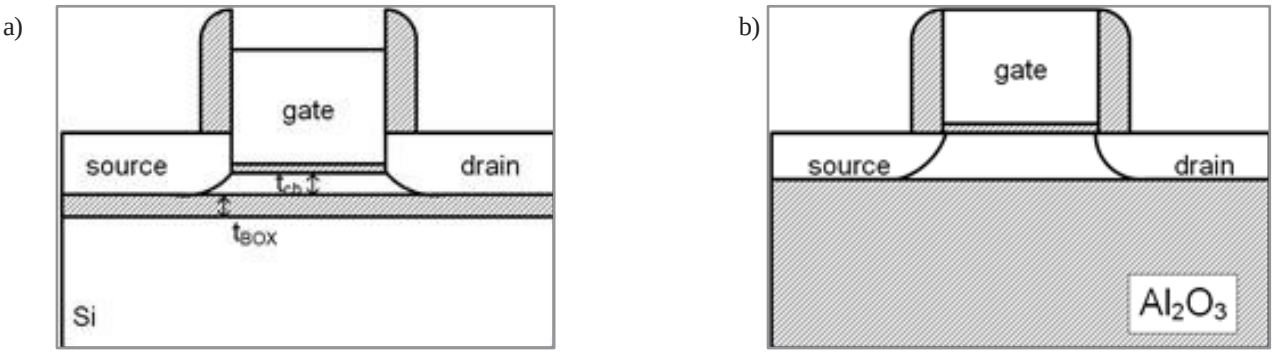

Figure 1: a – Ultra-Thin-Body-and-BOX Transistors on Silicon Dioxide Insulator (UT BB) Structure; b – Ultra-Thin-Silicon Body on Sapphire Insulator (UTSi) Structure [2, 3].

UTBB SOI MOSFETs are most attractive devices for the next technology nodes. Thanks to the good control of short-channel effects they not only exhibit excellent analog and RF performances but also outperform bulk and FinFET technologies on various RF aspects.

However, two effects are critical for the operation of Ultra-thin SOI MOSFETs:

1. Self-heating because of the small thermal conductivity of the isolation layer (SiO2=0.2-1.4 W/m-K) in comparison with the silicon layer (λSi=84-140 W/m-K).
2. The coupling between the front and back channels making questionable the viability of traditional behavior of the device.

UTSi MOSFETs on SOS technology are attractive devices for low-power, ultra-high bandwidth communication RD ICs, highly integrated multimedia wireless systems based on the IEEE 802.11 standard and optoelectronic ICs for optical communication systems because the sapphire substrate is practically transparent in wavelengths ranging from the ultra-violet (200nm) to infrared (5500nm). The sapphire substrate is excellent electrical insulator, and its thermal conductivity ($\lambda_{sapphire}$=46 W/m-K) is higher than silicon dioxide. Moreover, the MOSFETs on SOS substrate are more temperature and radiation hardened than the devices on SOI substrate. Because of the minimal interaction between the components through the dielectric sapphire substrate the UTSi SOS MOSFETs are good candidates for the monolithic high frequency wideband performance ICs consisted of active transistors and passive higher-Q inductors, varactors and resistors.

However, in SOS MOSFETs the silicon body layer thickness is limited 100-80 nm. In the devices with thinner silicon body layer the leakage current is increased and the electron mobility in the silicon layer is decreased due to the high defect density in the epitaxial layer of silicon near the silicon-sapphire interface.

In order to fully realize the advantages of the Ultra-Thin-Body MOSFETs the comprehensive analysis of their characteristics using the computer modeling is necessary. For this purpose, two types of device models are used: 1) TCAD 2D/3D digital models for the detailed analysis of physical effects in device structures; 2) compact SPICE models to describe the electrical characteristics of the device for circuit simulation.

The sufficient works have been dedicated to the UTBB SOI modeling. The effectiveness of the different UTBB SOI MOSFET structures in managing the associated short-channel effects such as drain-induced barrier lowering (DIBL), subthreshold swing (SS), off-state leakage current (Ioff) and other physical effects has been investigated using TCAD models [4, 5]. Much research on the electrical characteristics of UTBB SOI using SPICE models has been published [6].

Unfortunately, few reports have been presented dealing with the behavior of UTSi SOS MOSFETs. So, in this paper a detailed study of DC and AC behaviors of UTSi SOS MOSFETS using TCAD and SPICE models is performed. The devices under test (DUT) are the Ultra-Thin-Silicon (UTSi) transistors fabricated by 0.5um pSemi (formerly Peregrine Semiconductor) special SOS CMOS process that grows 100nm silicon on top of fully insulating synthetic sapphire [7].

TCAD Modeling of UTSi SOS MOSFET

The typical Ultra-Thin Silicon-on-Sapphire n- and p-MOSFET with L/W=0.4/10 um and tSi=100nm were considered as DUTs. TCAD model of MOSFET SOS was developed. The impurity concentrations in the channel, drain and source were set in accordance with [8]. The cross section of the device is shown in Figure 1, b. The main physical and geometrical parameters: gate dielectric thickness – 10nm; active silicon layer thickness – 100nm; channel doping – 1.5E17 cm-3.

To simulate the electrical performance the following set of physical models, for submicron and deep-submicron MOSFETs, was used:

1. Enormal (IALMob, Coulomb2D) – model of surface mobility degradation with two-dimensional distribution of defects at the interface.
2. CarrierCarrierScattering (BrooksHerring) – model of mobility degradation due to scattering of carriers on other charge carriers.
3. DopingDependence (PhuMob) – a model of the dependence of mobility on the doping level, also including the consideration of the ballistic flight of carriers in short-channel transistors.
4. Slotboom – band gap narrowing model.
5. HighFieldSaturation – model of charge carrier mobility degradation in a strong field.
6. SRH (DopingDependence) – Shockley-Hall-Reed model of carrier generation-recombination considering the dependence of the recombination rate on the carrier concentration [9].

TCAD Model Verification

In Ultra-Thin SOS MOSFETs the electrical properties of the silicon-sapphire interface have a significant influence on the device characteristics, particularly the off-state source-drain leakage current Ioff. The charge-induced depletion at the silicon-sapphire interface is also conductive to source-drain punch through which would limit the maximum applicable drain bias.

So, in TCAD model of those devices two significant physical effects in the Ultra-Thin Silicon channel layer due to the high density of interface states must be considered. For the n- and p-silicon the presence of positive and negative trapped charges, respectively, is required. The simulations with fitted trapped charges for electrons and holes must be repeated to verify the experimental data. Analogously, using the fitting procedure for the carrier mobilities μn and μp, the lower effect of the saturation current Ion and transconductance gm can be considered.

In Figure 2 the input I-V characteristic of 0.4um UTSi SOS MOSFET with tSi=100nm are presented before and after verification.

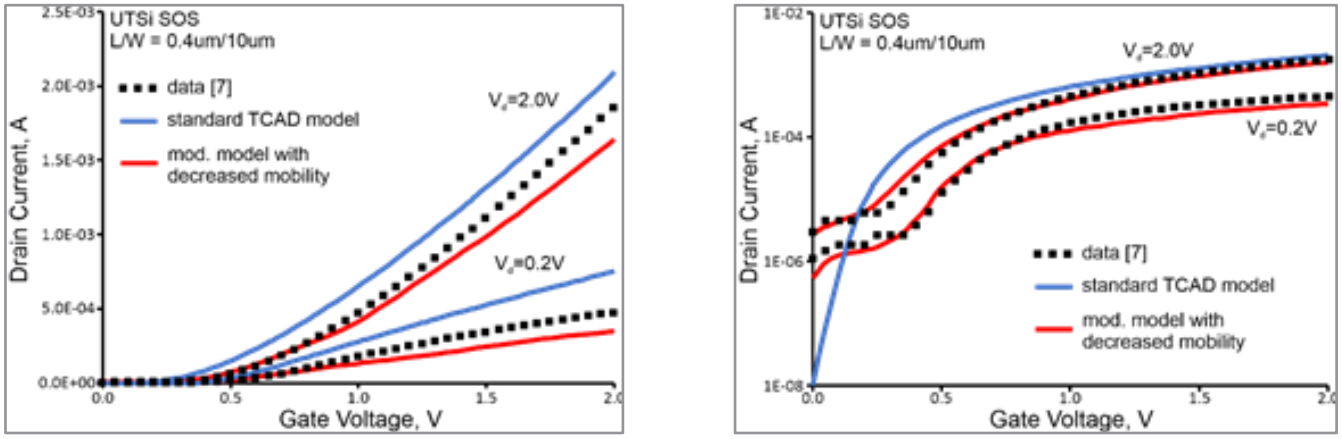

Figure 2: Comparison of IdVg simulation results with standard model, modified model and experimental data [7].

UTSi SOS MOSFET Structure with the Modified Channel

However, the UTSi SOS MOSFET technology with a topological size of 0.5 um and less requires the manufacturing equipment modernization. In our work the new design of SOS MOSFET allowing to increase the transistor dynamic characteristics to 20-40% without significant capital expenditures for the modernization of production capacities is investigated [10].

The design feature is the presence of high-resistance undoped silicon of intrinsic conductivity ("insertion") in the channel region near the source (see Figure 3). The area provides a significant decrease in the threshold voltage, an increase in channel conductivity, and, consequently, an increase in performance. The doping profile example for the intrinsic conduction region length Xp = 50%·is presented in Figure 4.

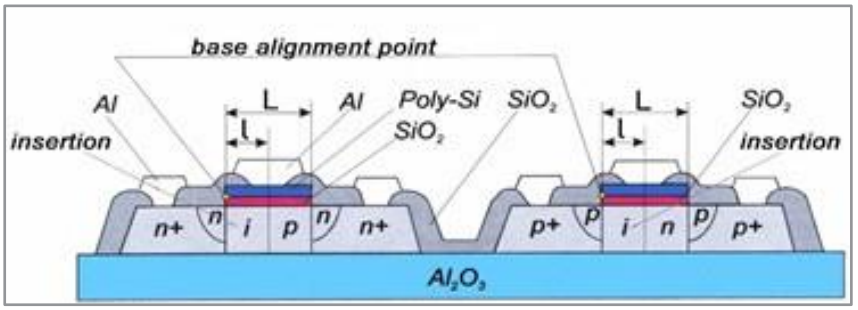

Figure 3: CMOS structure with the insertion of intrinsic conductivity area in a channel [10].

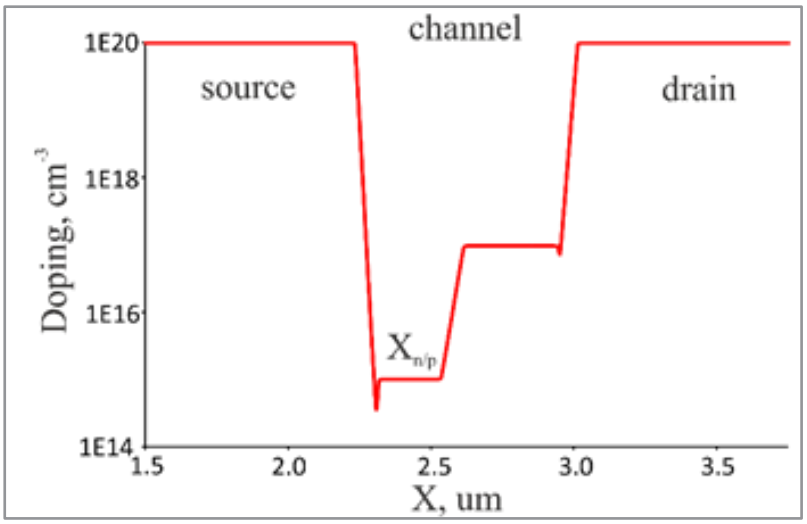

Figure 4: Doping profile with intrinsic conduction region length 50%.

The current-voltage characteristics were simulated in two regimes: OFF (Vds=0.1 V, Vgs varies from 0 V to 3.5 V) and ON (Uds=3.5 V, Vgs varies from 0 V to 3.5 V). Dynamic characteristics were simulated on the CMOS cell consisting of the corresponding n- and p-channel MOSFETs.

At the first stage, 0.75 um UTSi SOS MOSFET structure was simulated and its main parameters (threshold voltage Vth, saturation current Ion and leakage current Ioff) are compared with the standard design. Then, the main parameter dependences on the intrinsic conductivity area size were investigated. Finally, an evaluation of the increase in performance was carried out.

The 0.75 um structure with a thin active layer (tSi=0.1 um) has a lower threshold voltage (by 21%) and a large saturation current (1.4 times), while the leakage current increased slightly and remained at level ~1·10-13 A.

However, when the intrinsic conductivity area size is more than half the channel length, there is a significant increase in leakage current in the OFF regime by 4 orders (~nA) and in the ON regime by 8 orders (~0.1 mA). This negatively affects the functioning of the device in the ON regime. It negatively affects the device functioning in the ON regime. The most optimal parameter set corresponds to the intrinsic conductivity area size of 25% (see Figure 5 and Figure 6).

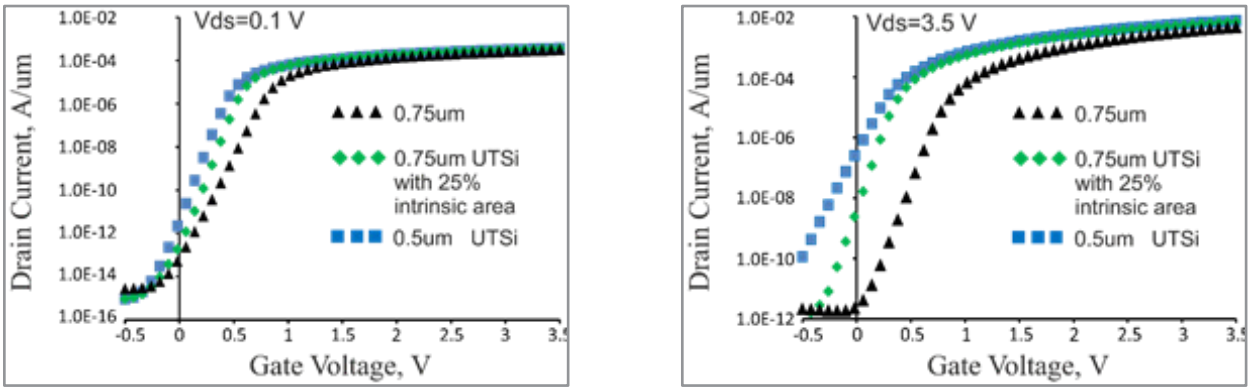

Figure 5: Comparing simulated IdVg n-channel UTSi 0.75 um SOS MOSFET (Xp=25%) characteristics with UTSi 0.5 um

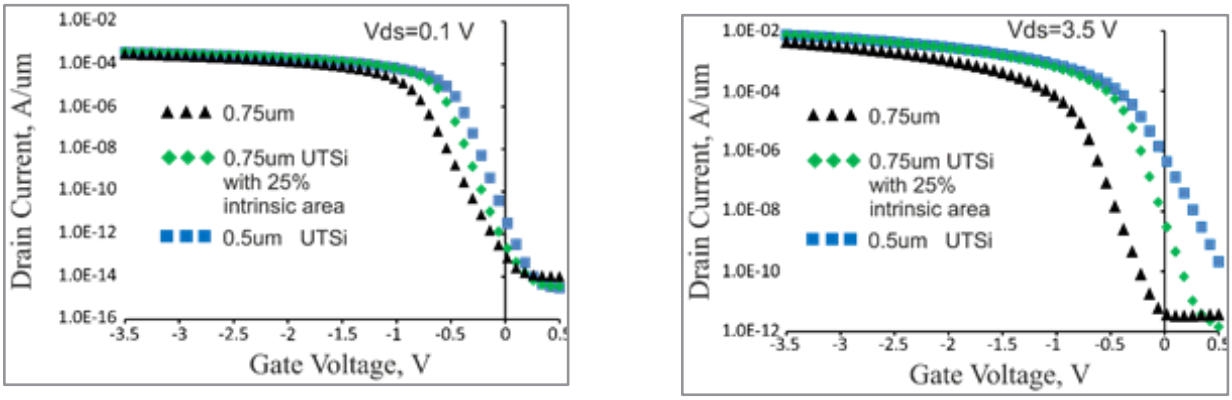

Figure 6: Comparing simulated IdVg p-channel UTSi 0.75 um SOS MOSFET (Xn=25%) characteristics with UTSi 0.5 um

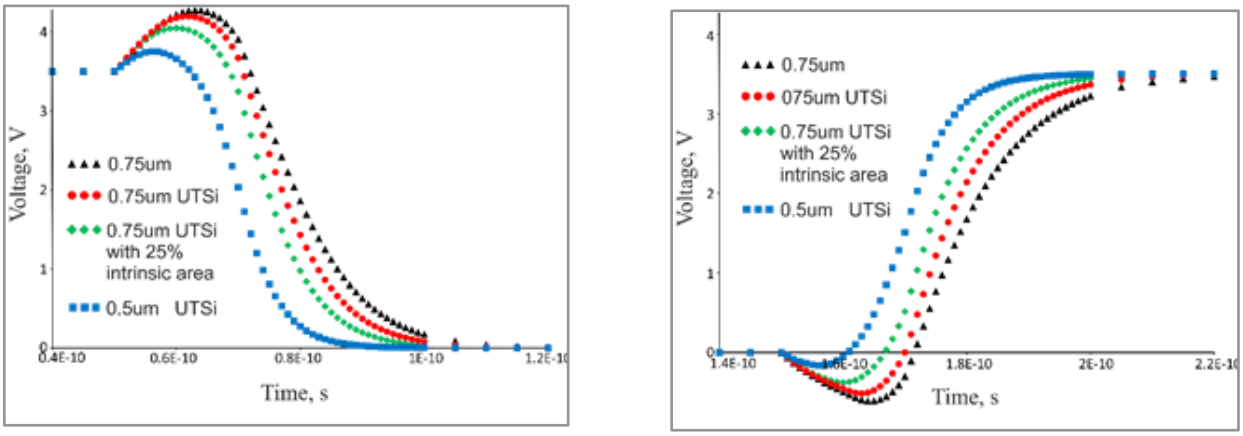

Figure 7: Simulated transient characteristics of CMOS cells

Compared with the traditional 0.75 um technology (see Table 1-3), it is possible to achieve an increase in performance by 2 times. However, as mentioned above, when the intrinsic conductivity area size is more than half the channel length, the significant leakage current is observed. In this way, the most optimal parameter set corresponds to the intrinsic conductivity area size of 25%. In this case, delay time decreases by 26%.

Table 1: Simulated 0.75 um SOS n-MOSFET main parameters

	SOS MOSFET Traditional				SOS MOSFET UTSi			
Xp/n	0	25%	50%	75%	0	25%	50%	75%
Vth, V	0.94	0.92	0.86	0.68	0.74	0.68	0.62	0.46
Ioff_OFF, A	5.3E-14	1.1E-13	2.2E-13	2.1E-11	7.3E-14	1.8E-13	9.5E-13	2.1E-09
Ioff_ON, A	2.29E-12	4.39E-10	5.75E-06	6.8E-04	2.29E-12	4.39E-10	5.75E-06	6.8E-04
Ion, A	4.54E-03	5.17E-03	6.21E-03	9.20E-03	6.04E-03	6.74E-03	7.29E-03	8.48E-03

Table 2: Simulated 0.75 um SOS p-MOSFET main parameters

	SOS MOSFET Traditional				SOS MOSFET UTSi			
Xp/n	0	25%	50%	75%	0	25%	50%	75%
Vth, V	-0.88	-0.86	-0.82	-0.6	-0.7	-0.66	-0.59	-0.45
Ileak_OFF, A	2.6E-14	1.5E-13	3.0E-13	3.9E-11	8.79E-14	2.12E-13	1.09E-12	2.9E-09
Ileak_ON, A	3.70E-12	9.60E-10	1.24E-05	1.00E-03	7.17E-12	2.96E-09	8.74E-06	3.98E-04
Ion, A	4.30E-03	5.02E-03	6.33E-03	1.03E-02	6.36E-03	7.34E-03	8.16E-03	9.96E-03

Table 3: Simulated delay time for 0.75 um CMOS cell

	SOS MOSFET Traditional		SOS MOSFET UTSi	
Xp/n	0	25%	0	25%
tdelay01, ps	21.1	17.8	17.6	15.0
tdelay10, ps	20.4	18.2	18.3	15.8

The design of 0.75 μm SOS MOSFET with the use of high-resistance undoped silicon of intrinsic conductivity ("insertion") in the channel region near the source makes possible to obtain the transistor with parameters and characteristics corresponding to a transistor with a topological channel length of 0.5 um. This allows the factories to produce new competitive products without significant capital expenditures for the modernization of production capacities.

SPICE Modeling of UTSi SOS MOSFETs

The special compact model of UT SOI MOSFET for circuit design of VLSIs using SPICE-like simulators was developed, considering the electro-physical in properties Ultra-Thin silicon device structure [8].

The main advantage of UT SOS MOSFETs in the capability of reliable behavior in the ultra-wide temperature range: in low-temperature (−269…+100°C) and high-temperature (−60…+300°C). Based on the requirements for the application, the models are subdivided, respectively, into two groups: low- and high-temperature.

SPICE Modeling Methodology

The temperature wide range version of UT SOI model was not earlier developed. For this purpose, the standard SPICE model UTSOIv.2 was chosen as a core model: for 250- and 500-nm SOS MOSFETs fabricated by UTSi CMOS process with silicon film thickness TSI = 100 nm. The core model was then complemented with additional approximating expressions for temperature-dependent parameters and/or with external standard circuit components (for the cases where internal model parameters do not allow to solve the problem alone) [11, 12].

Drain current equation in the UTSOI standard model is as follows:

$$I_{DS} = \beta(UO) \cdot F_{\Delta I}(A1O, A2O) \times \times \frac{q_{in}^{*}}{G_{TSAT}(THESATO)} \cdot \Delta\psi(VFBO) \quad (1)$$

The temperature-dependent model parameters of the UTSOI are threshold voltage-related (VFBO), carrier mobility-related (UO, MUEO, THEMUO), velocity saturation (THESATO), series resistance (RS), Coulomb scattering (CSO), DIBL-effect related (CF), impact ionization current-related (A1O, A2O) and others.

Several parameters of the initial models use the built-in dependencies on temperature, while new or refined dependencies were introduced for a number of parameters.

In high and low temperature ranges the parameters RS, DIBL-effect parameters CF and velocity saturation THESATO change in accordance with the polynomial functions:

$$\Delta p_i(T) = a_0 + a_1 \cdot \Delta T + a_2 \cdot \Delta T^2 + \ldots \quad (2)$$

The dependence of the threshold voltage-related parameters VFBO are expressed by the exponential function:

$$\Delta p_i(T) = b_0\left[\exp\left(b_1\cdot\Delta T + b_2\cdot\Delta T^2 + \ldots\right) - 1\right] \quad (3)$$

To take into account the behaviour features of carrier mobility-related parameters UO, MUEO, THEMUO at high and low temperatures, new analytical dependencies were introduced in these models, giving a small error in the high and low temperature range [13].

$$p_i(T) = p_i(T_{nom})\cdot\left(\frac{T}{T_{nom}}\right)^{c_0 + c_1(T/T_{nom}) + c_2(T/T_{nom})^2 + \ldots} \quad (4)$$

In (3)– (5) ai, bi, ci are the fitting coefficients, T – temperature in Kelvins. The built-in temperature coefficients of the base models should be set to zero.

To additionally account for the kink effect that appears in SOS MOSFETs in the cryogenic range due to the carrier freeze-out effect, we used the following subcircuit approach. Figure 8,a presents the equivalent circuit of additional voltage-controlled voltage source VG_COR connected in series to the gate contact to emulate freeze-out of the substrate [14].

VG_COR (VDS, VGS) is a complex function of the drain-source VDS and the gate-source VGS voltage, which can be written as:

$$\frac{DV}{1+\exp\left[b\cdot\left(p_0 + p_1\cdot V_{GS} + p_2\cdot V_{GS}^2 - V_{DS}\right)\right]} \quad (5)$$

where DV, b, p0, p1, p2 – fitting factors.

The procedure for determining the fitting factors of VG_COR (VDS, VGS) is illustrated by the example of measured output I-V characteristics of SOS n-MOSFET [7] at the temperature 4.2 K, which shows the manifestation of kink effect.

Factors p0, p1, p2 of (5) can be determined by means of inspecting and fitting the kink pinch-off voltage shift with gate bias on the output MOSFET curves (see Figure 8,c). The slope of characteristic at the kink start points can be fitted by factors DV and b. The results of modeling using the proposed sub-circuit model with and without account for kink effect are shown in Figure 8,b.

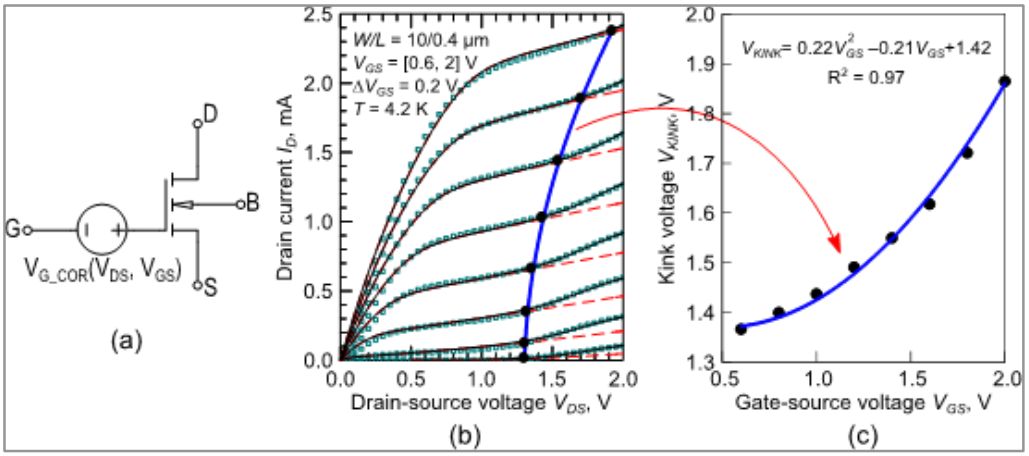

Figure 8: Schematic representation of the subcircuit model to account for the kink effect in MOSFETs (a); assessment of coefficients for the VG_COR(VDS, VGS) dependency: experimental data [7] (symbols), simulation with (solid lines) and without (dashed lines) account for the kink effect (b); fitting the Vkink(VGS) dependency (c)

Model Parameter Extraction Procedure

The model parameter extraction procedure in the wide temperature range is automated with industry extraction tool IC-CAP, which simplifies data exchange and processing.

The initial data are the sets of IV and CV-curves of standard semiconductor devices of different sizes, obtained as a result of measurements or process and device simulation for different values of temperature and transmitted to IC-CAP using an in-house software interface. The extraction procedure allows obtaining model parameters for intermediate temperature values and includes the Following Steps:

- **Step 1.** Determination of the complete set of model parameters on the basis of measurement data obtained at room temperature. The method used to identify the parameters includes a combination of analytical and optimization procedures.
- **Step 2.** A list of main temperature-dependent parameters is selected from the complete set of parameters.
- **Step 3.** For each temperature value Ti, the corresponding values of the selected model parameters are determined based on the measurement results. This procedure is automatically repeated for all planned discrete values of temperature Ti: i = 1…n.
- **Step 4.** The temperature dependencies of the model parameters obtained in step 3 are approximated by analytical functions of the form [2, 4].

The coefficients of such functions constitute a set of temperature parameters of the entire model. Precise adjustment of the values of the temperature parameters is made using global optimization, i.e. for all available experimental characteristics.

- **Step 5.** The resulting analytical expressions together with the coefficients are built into the description of the SOS MOSFETs SPICE model, that is further included in the library of models.

Model Verification

As an example for SOS MOSFET modeling in the low-temperature range, the UTSOIv.2-based model parameters were identified for a n-channel SOS MOSFETs with W/L = 10/0.25 um fabricated by the Peregrine 250-nm Silicon-on-Sapphire CMOS process using the described extraction procedure. The structure parameters are: tSi = 100 nm, tox = 10 nm. Figure 9 show output I-V characteristics in the temperature range −269°C…+27°C: measured and simulated on the basis of the developed model [7]. Figure 10,a,b shows a comparison of measured and simulated output I-V characteristics for a 500-nm n-SOS MOSFETs with W/L = 10/0.4 um by the Peregrine at T = 27°C and T = –269°C.

As an example, for high temperature in Figure 10,c a comparison of measured and simulated SOS n-MOSFET with W/L = 800/16 um transconductance efficiency (gm/ID) vs. normalized inversion coefficient (IC0) in the temperature range T = 25…300°C is shown [15].

The modeling error of the current-voltage characteristics is 8-12% in the low and high temperature ranges.

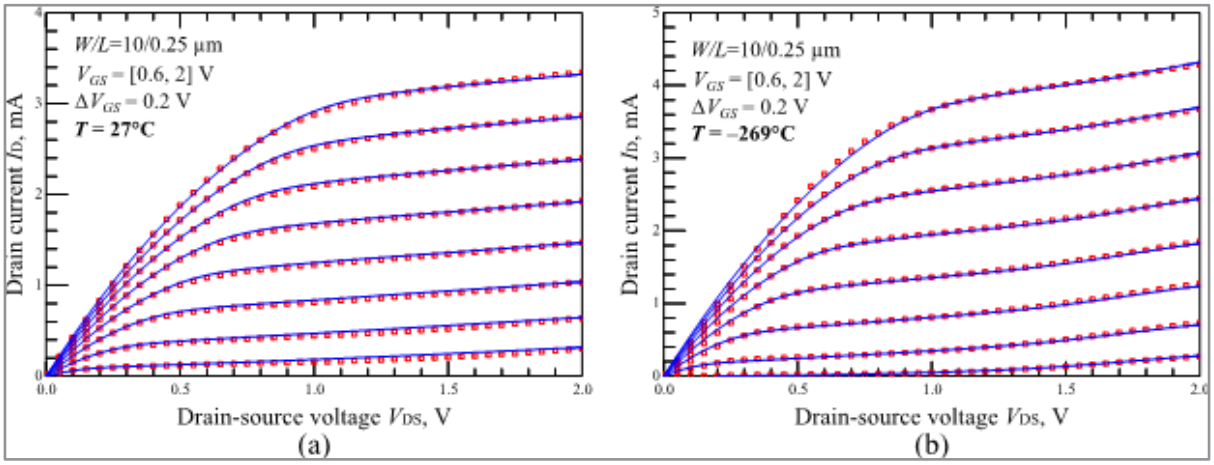

Figure 9: Measured and simulated output IV-characteristics of n-channel SOS MOSFET with W/L = 10/0.25 um from the Peregrine 250-nm SOS CMOS process at 27°C (a) and -269°C (b) (symbols—measurements [7], lines—simulation)

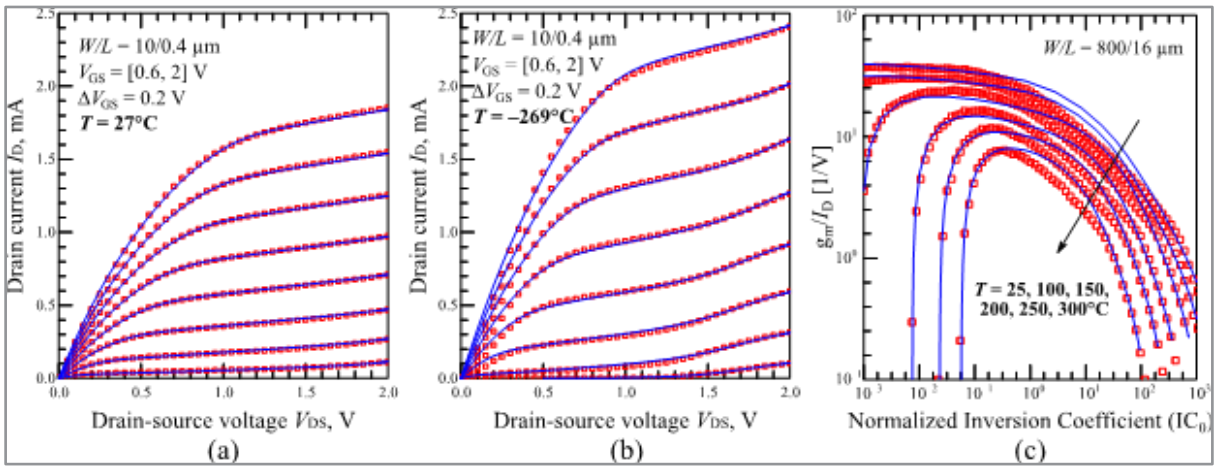

Figure 10: Comparison of the measured data (symbols) and the SPICE-simulation results (lines) of 500-nm SOS n-MOSFET output I-V characteristics at T = 27°C (a) and T = –269°C (b) [7]. Measured (symbols) and simulated (lines) SOS n-MOSFET transconductance efficiency (gm/ID) vs. normalized inversion coefficient (IC0) in the temperature range T = 25…300°C (c) [15].

Conclusions

Peregrine Semiconductor Ultra-Thin Silicon on Sapphire CMOS is one of the most challenging technology for multimedia wireless communication high integrated, ultra-high wideband RF ICs. This ICs grow rapidly for civil and special space and military systems working in the extremal conditions under tempera-

ture and radiation influence. To fully realize the advantages of the UT SOS CMOS circuits the computer TCAD and SPICE modeling is necessary.

Unfortunately, the high potentialities of the TCAD and SPICE models with have been developed for the conventional MOSFETs were not completely realized for the UT Silicon-on-Sapphire transistor structures.

The following novelties were introduced in TCAD modeling of UT SOS MOSFETs:

1. Two physical effects: trapped charge density growing and carrier mobility lowing in the thin silicon channel layer due to the high density of interface states on "Silicon-on-Sapphire" were included in to carrier transport model.
2. The novel UT SOS MOSFET structure with high-resistance undoped silicon region near the drain was considered. It was shown that the delay time of CMOS invertor based on these devices is 25% lower in comparison with conventional CMOS.

The following novelties were introduced in compact SPICE modeling:

1. Extended version of SPICE UT SOI model of SOI/SOS MOSFET was at first developed considering the super-wide temperature range (-260ºC…+300ºC). The simulation error of the static IV characteristics was not more than 10%-20%.
2. Special sub-circuit was added into standard MOSFET model to account for kink effect.

Acknowledgment

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