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FPGA-Based Bridge Stress Structure Detection System

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Abstract
vibrating string sensors are widely utilized in bridge stress monitoring systems because of their high preci-sion and robustness in measur¬ing structural strain and stress. This paper proposes an advanced bridge stress monitoring system based on field-programmable gate arrays (FPGAs) and advanced RISC machines (ARMs) as core pro¬cess-ing units, enabling efficient and reliable operation. The system architecture com-prises four integral subsystems: a data acquisition module, an FPGA-based data processing unit, a data transmission framework, and a comprehen-sive data management subsystem. The FPGA subsystem, im-plemented via the Altera Cyclone IV EP4CE10E22C8N device, integrates critical modules, including an excitation signal generator, a sweep signal controller, a frequency meas¬urement unit, and a top-level sys-tem coordinator. These modules collectively enable precise frequency signal measurements from vibrat¬ing string sensors, achieving a measurement accuracy of 99%. The ARM subsystem, which is based on the STMicroelectronics STM32F407 microcon¬troller, manages data communication protocols, system-level control operations, and user interface interactions, ensuring seamless hardware–software integration. The experimental results demonstrate that the proposed system exhibits high stability, reliability, and strong resis-tance to interference. These attributes make it highly suitable for practical applications in bridge stress monitoring. The system's modular design and scalable architec¬ture further enhance its adapt-ability to various monitoring requirements, offering valuable insights for engineers and researchers in the field of structural health monitoring. This work provides a robust reference for the development of intelli-gent transportation systems and large-scale infrastructure monitoring applications.

Keywords: Bridge Stress, FPGA, ARM, Vibrating Wire Sensor

Introduction

With the development of the social economy, bridge construction in China has achieved remarkable ac-complishments. However, influenced by external environmental factors, bridge structures inevitably suffer damage and destruction, drawing significant attention to bridge structural health from society. Bridge dis-asters not only cause severe losses to the environment, resources, and property but also endanger people's life and property safety. This paper combines the development of domestic and interna-tional bridge tech-nologies with the application of electronic monitoring systems to establish a remote monitoring system for bridge stress structures, aiming to monitor the health conditions of bridges and provide a basis for mainte-nance and prevention work. The following section analyzes the composition of the bridge stress structure remote monitoring system.

To visualize bridge stress structure data and strengthen the mon-itoring of bridge health condi¬tions, this study designs a remote monitoring sys¬tem for bridge stress structures based on vi-brating wire sensors, as shown in Figure 1. The system primarily con¬sists of a data acquisition subsystem, a data processing sub-system, and a data management and transmission subsystem.

Design of a Remote Monitoring System for Bridge Stress Structures

Bridge stress monitoring system

To achieve the digitization of bridge stress structure data and assess bridge health status, a remote moni-toring sys¬tem based on vibrating string sensors was developed. As illustrated in Fig-ure 1, the system com-prises a data acquisition subsystem, a data processing subsystem, and a data management and transmis-sion subsystem. This design ensures precise and reliable monitoring capabili¬ties [1].

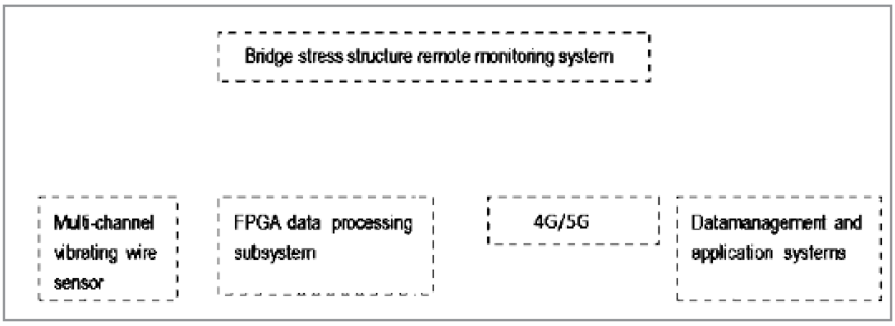

Figure 1: bridge Stress Monitoring System Block Diagram

Vibrating Wire Sensor

The vibrating string sensor operates on the principle that the frequency of a rigid string changes in re-sponse to the stress applied to the steel wire, enabling the precise measurement of stress variations in bridge structures. This sensor out¬puts a fre-quency signal characterized by strong anti-interfer¬ence capabi-li-ties and the ability to transmit over long distances, making it highly suitable for bridge stress monitoring applications. From a structural perspective, vibrating string sensors lack moving components, increasing their durability and reliability. During operation, the vibrator requires exter¬nal excitation owing to inherent damping effects and energy dissipation during vibra-tion. As depicted in Figure 2, the system's operational principle involves an excitation signal prompting the vibrator to oscillate.

A detection element captures the resulting frequency signal, which is subsequently fed back to the excita-tion circuit through an am-plification process. The vibrating string within the sensor experi-ences varying forces, consequently altering its emitted frequency. By applying a series of distinct frequencies to induce resonance in the vibrating string, the corresponding frequency value can be measured and utilized to cal-culate the force exerted on the sensor. This method ensures accurate and reliable stress measurement, which is crucial for effective bridge monitoring systems.

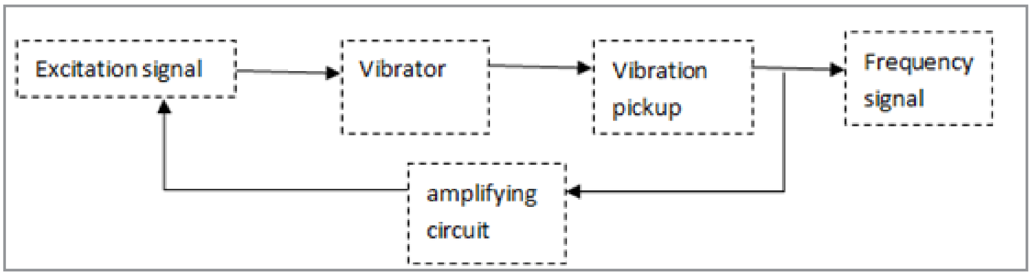

Figure 2: Sensor working principle block diagram

FPGA Data Processing System

Vibrating Wire Sensor

The vibrating string sensor measures the frequency of string vibrations, which requires an initial excitation process. Two primary excitation methods are commonly employed: the first involves applying an instan-taneous high-voltage, high-current pulse to the sensor, which necessitates the design and imple-mentation of a boost circuit to amplify the driving signal. The second method leverages the resonance principle, which is more efficient and energy-effective. In this study, we adopt the res-onance-based excitation tech-nique, which uses an FPGA pro-cessor to generate a precisely controlled square wave signal. By tuning the frequency of this square wave signal to closely align with the natural oscillation frequency of the sensor's vibrat-ing string, resonance is effectively induced. Once resonance is achieved, the excitation signal is re-moved, and the sensor emits a characteristic frequency signal. This signal is then processed by the system to accurately determine the fundamental frequen-cy of the vibrating string sensor. The measured frequency is sub-sequently used to calculate the mechanical stress imposed on the monitored bridge structure. This approach not only enhances the precision and reliability of stress measurements but also demonstrates the potential of FPGA-based systems in advanced sensor applications [2].

Data Processing System

The data processing system employs an Altera FPGA, specifically the EP4CE10E22C8N programmable logic controller, to implement a resonance-based frequency measurement system for multiple vibrating string sensors. To achieve this functionality, four state machine modules are developed in the software: the excitation signal module, the sweep signal module, the frequency measurement signal module, and the top module. These modules are integrated into a cohesive architecture to enable precise frequency meas-urement of vibrating string sensors. A detailed illustration of the software structure is provided in Figure 3.

The excitation signal module plays a pivotal role in controlling the timing of the excitation process and issuing control instructions to both the frequency measurement module and the sweep module. This en-sures synchronized operation of the system components. The sweep module is responsible for generating and transmitting sweep signals across a range of frequencies. These signals are continuously adjusted on the basis of predefined base data and incremental frequency steps, known as sweep increments. Im-portantly, the sweep increment is dynamically regulated by an ARM processor, specifically the STM32F407 microcontroller, enabling fine-tuned control over the frequency sweep process. The frequen-cy measurement module serves as the core component for capturing and analyzing sensor data. It receives control signals from both the excitation module and the sweep module to initiate frequency measurements. By processing these inputs, the module accurately determines the frequency data of the vibrating string sensor. This integrated approach ensures that the system operates efficiently, providing reliable and precise measurements for applications requiring high accuracy in structural monitoring.

Sensor Acquisition Drive System

In Figure 3, the system is designed to accommodate 16 sensors and employs sweep frequency signals to facilitate precise frequency measurement. Sweep frequency signal generation is a critical component of the system, as it drives the Darlington transistor to produce a high-frequency and high-voltage excitation pulse signal. This pulse signal is then used to excite the vibrator, initiating the vibration of the string within the sensor. As a result, the vibrating string generates a measurable frequency signal, which forms the basis for subsequent analysis.

However, the signal produced by the vibrating string sensor is inherently weak and requires preprocessing to ensure accurate measurement. To address this, the system incorporates filtering, amplification, and shaping circuits to perform signal conditioning. These circuits work in tandem to increase the quality of the signal, eliminate noise, and prepare it for further processing. The filtering stage removes unwanted in-terference, whereas the amplification stage increases the signal amplitude to an appropriate level for measurement. Finally, the shaping circuit ensures that the signal has a consistent and well-defined wave-form, which is essential for precise frequency determination.

After the frequency measurement module processes the conditioned signal, the resulting frequency data are transmitted to the top-level module of the FPGA-based data processing system. This top-level module acts as the central hub for data interaction, coordinating communication between the FPGA and the exter-nal data transmission system. The external data transmission system is implemented via an ARM processor (STM32F407), which is responsible for managing and disseminating the processed data. Specifically, the bridge stress data derived from the frequency measurements are transmitted to facilitate effective bridge system management and maintenance [3].

This integrated approach ensures that the system operates efficiently and reliably, enabling accurate moni-toring of bridge stress levels. The combination of FPGA-based signal processing, ARM processor-driven data transmission, and advanced signal conditioning circuits highlights the system's ability to handle com-plex tasks in real time while maintaining high precision and robustness. This design is particularly valua-ble for applications requiring continuous and precise structural monitoring, such as bridge health assess-ment and maintenance optimization.

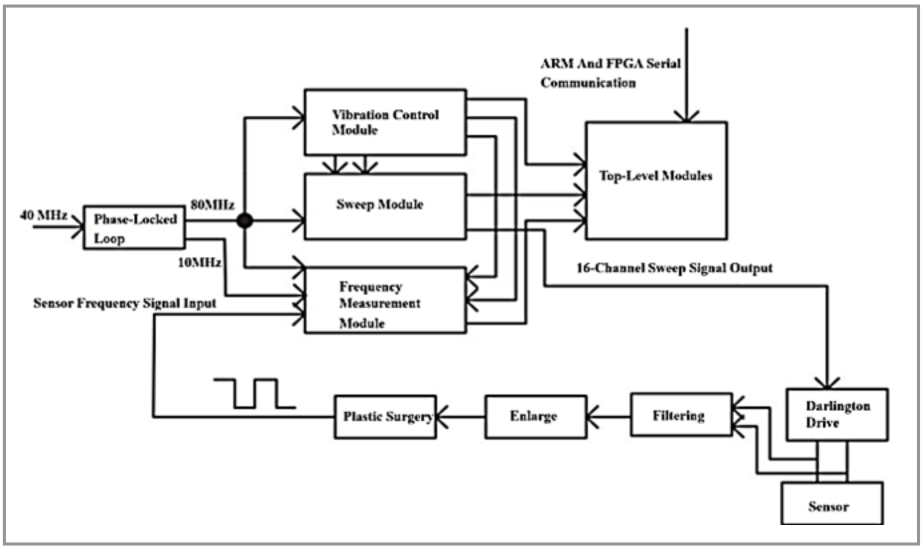

Figure 3: FPGA data processing structure diagram

Data Mgmt & Trans System

Transmission System

The data transmission system is built around the ST's ARM processor, specifically the STM32F407 micro-controller, to ensure robust and efficient data handling. The system primarily utilizes a parallel communi-cation bus to facilitate seamless data transfer and processing between the FPGA and ARM modules. This interface allows for high-speed data exchange, ensuring minimal latency and maximal throughput. Addi-tionally, the system is equipped with wireless connectivity features, enabling it to interface with 4G/5G mobile networks and remote data centers. This setup ensures that data can be transmitted wirelessly over long distances with high reliability, making it suitable for real-world applications where physical proximity may not always be feasible [4].

Furthermore, the data transmission system incorporates a user-friendly interface that supports system con-figuration and human–computer interaction. This feature allows operators to adjust system parameters, view real-time data, and monitor the status of ongoing processes. The ability to display relevant data in real time enhances the system's usability and aids in decision-making during operations. By integrating these advanced functionalities, the data transmission system not only achieves its primary objective of re-liable data transfer but also provides a comprehensive platform for system management and maintenance.

Management System

The data management system is designed to comprehensively oversee and analyze the entire spectrum of bridge-related data, ensuring the integrity and safety of bridge structures. The system is equipped with ad-vanced monitoring capabilities, enabling it to track dynamically and assess changes in both structural in-tegrity and stress levels in real time. When significant deviations or anomalies in bridge stress are detected, the system immediately triggers an alarm mechanism, forwarding critical alert signals to relevant stake-holders. This proactive approach aims to prevent potential structural failures caused by excessive stress, thereby mitigating the risk of catastrophic events such as bridge collapse. By doing so, the system plays a pivotal role in safeguarding public safety and minimizing societal disruption [5].

Moreover, the data management system ensures the secure and efficient storage of all collected bridge da-ta. These stored records serve as a cornerstone for subsequent analytical processes, including stress evalu-ation, structural health assessment, and maintenance planning. By leveraging historical and real-time data, the system facilitates the identification and mitigation of potential stress-related hazards, ensuring the long-term reliability and resilience of bridge infrastructure. This robust framework not only enhances the operational efficiency of bridge management but also contributes to sustainable infrastructure devel-op-ment.

In summary, the data management system represents a critical component in modern bridge monitoring and maintenance systems. Its ability to integrate real-time monitoring, alarm generation, and data analytics ensures a holistic approach to bridge safety and durability. By providing actionable insights and enabling timely interventions, the system effectively addresses the societal impacts associated with bridge failures, ultimately fostering safer and more resilient infrastructure for communities worldwide [6].

Hardware Experimental Platform Construction

This dual-core measurement system, which is based on FPGA EP4CE10E22C8N and ARM STM32F407, achieves precise frequency acquisition for vibrating wire sensors. The architecture comprises three core modules:

1. Excitation Control Module: Timing control of excitation waveforms through state machines
2. Frequency Sweep Output Module: Resonance point search with configurable parameters
3. Frequency Measurement Module: High-frequency signal acquisition via the period measurement method

Excitation Control Module

State Machine Design: As shown in Table 1, the mo- schedule controls measurement start/stop through the meas_str/meas_stp signals, with a state switching response time <800 ns2. Signal-Tap Verification: Figure 4 Waveforms demonstrating strict synchronization between the interrupt signal (INT) and meas_cnt, con-firming timing reliability.

Table 1 Excitation control signal specifications

Port Pin	Signal Specification
meas_str	Measurement Start: Trigger Signal to Frequency Measurement Module
meas_stp	Measurement Stop: Termination Signal to Frequency Measurement Module
meas_end	Measurement Completion: Acknowledgment from Frequency Measurement Module
meas_error	Measurement Error: Fault Indication from Frequency Measurement Module
swp_str	Sweep Initiation: Trigger Signal to Sweep Module
swp_stp	Sweep Termination: Reset Signal to Sweep Module
swp_add	Frequency Increment: Step Command to Sweep Module
swp_to_fmax	Maximum Frequency Reached: Status Update from Sweep Module

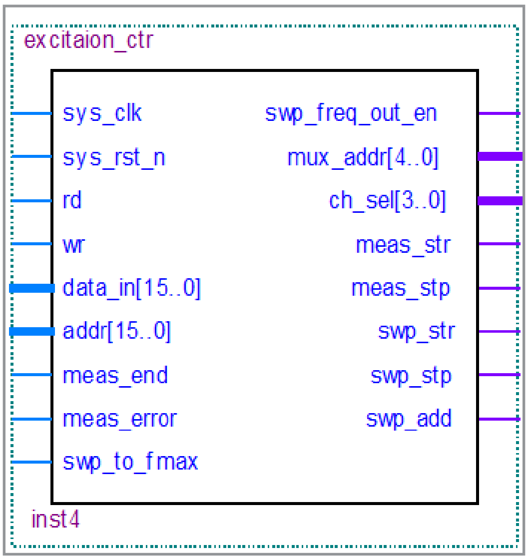

Figure 4: Excitation Control Module

Generation of the Sweep Frequency Output Module

Scanning signals excite the resonance of the vibrating wire sensor, enabling precise frequency measure-ment. As illustrated in Figure 5, the FPGA configures the scanning parameters as follows:

Initialization phase

- The channel lower limit register (0x3E8) sets the starting frequency to 1000 Hz (decimal equivalent of 0x3E8).
- The frequency increment (0x20) defines a step size of Hz for progressive scanning.

Adaptive Scanning Process

- The FPGA initiates frequency scanning from the lower limit and increases the output frequency iteratively until resonance is detected.
- Upon detecting resonance (characterized by abrupt amplitude changes in the sensor signal), the FPGA immediately triggers the frequency measurement module.
- If no resonance occurs, scanning continues until the predefined upper limit is reached.

Dynamic parameter configuration:

- Critical parameters, including the sweep range (lower/upper limits) and step size, are dynamically config-ured by the ARM via a 16-bit data bus. This flexibility accommodates diverse sensor types and environ-mental conditions.

Key signal definitions (see Table 2):

- sweep_start: Activates the scanning process.
- sweep_step: Controls frequency increment steps.
- resonance_detected: Flag indicating successful resonance identification [7].

Table 2 Sweep frequency signal descriptions

Port Pin	Signal Description
addr[15..0]	Address Signal
ch_sel[3..0]	Channel Selection Signal
data_out[15..0]	Data Output Signal
meas_error	Measurement Error

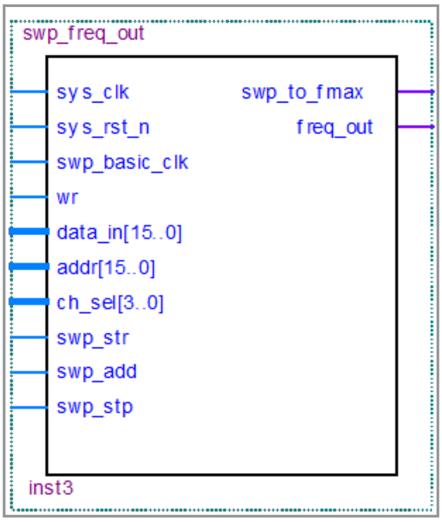

Figure 5: Sweep Frequency Output Module

Measurement Module

Frequency Measurement Method: This approach determines frequency f by counting the number of pulses N within a fixed gate time Tg (e.g., 1 second) and applying the formula: f=N/Tg

Period measurement method: To address limitations in short-duration signal measurement, the period method calculates frequency f by measuring clock pulses N within one signal cycle, deriving the peri-od T=N×Tclk, where Tclk is the (FPGA clock period, computing f=T/1.

- With Tclk=12.5 ns (80 MHz clock) and N=89212, the measured frequency becomes:
- f= 80×106/89212≈896.74 Hz (error±0.0011%)
- Experimental validation reveals an actual error of ±0.03%±0.03%, attributed to signal edge jitter and FPGA timing path delays.

Module features

- The functional implementation and pin connections are depicted in Figure 6.comprising the following key elements. Input synchronization eliminates metastability risks of freq_in using dual flip-flops, ensuring synchronization with sys_clk. Period Counting counts system clock pulses within one signal cycle via the precision measurement principle (f=N×fclk/T). Error Handling.Overflow detection: Checks whether the count exceeds predefined thresholds. No-Signal Detection, Triggers error flags via timeout counters. Con-trol Logic,
- The measurement is initiated by meas_str, with two rising edges capturing a single cycle duration [8].

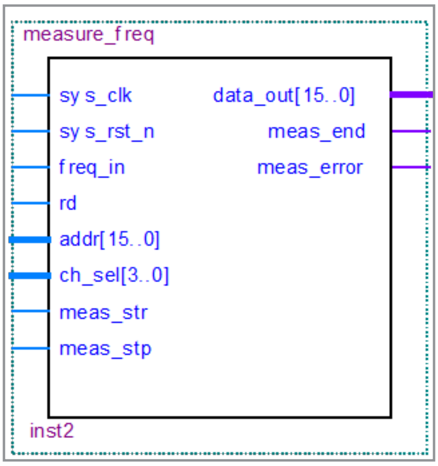

Figure 6. Measurement Module

FPGA–ARM Communication Protocol

To enable data interaction and control between the FPGA processor and the ARM microcontroller, we de-fine the following communication protocol. The ARM interface specifications for FPGA-ARM data ex-change include a 16-bit data bus, read control line, write control line, address bus, and interrupt line, as outlined in Table 3.

Table 2 ARM Interface Specifications

Name	ARM Pin
Data bus	P0.26~P0.10(P0.10 LSB)
Address bus	[P1.31,P1.29-P1.27,P1.20-P1.25,P1.18] (P1.18 LSB)
Read control	P1.16(High level)
Write control	P1.17(High level)
Interrupt	P0.30(Rising edge)

Experimental Results and Testing

Under normal operating conditions, the three sensors exhibit the following resonant frequencies:

Earth pressure cell: 1338 Hz, Piezometer: 2250 Hz, Displace-ment meter: 896 Hz. These frequencies are used to excite the sensors. During resonance, a distinct string vibration sound is observed. The measure-ment results demonstrate that the dis-placement meter produces the largest sinusoidal amplitude af-ter exci-tation. For visualization, an embedded logic analyzer (SignalTap) is employed to retrieve data via JTAG and display it on a computer. The frequency is calculated as f=800 000 000/meas_cntf, where meas_cnt represents the cycle count of the in-put frequency signal. Upon completion of the meas-urement, the FPGA generates an interrupt signal to notify the ARM processor to read the frequency data. Both meas_cnt and the interrupt sig-nal are successfully captured by the embedded logic analyzer (Signal-Tap), and the ARM reliably detects the interrupt, as il-lustrated in Figure 7.

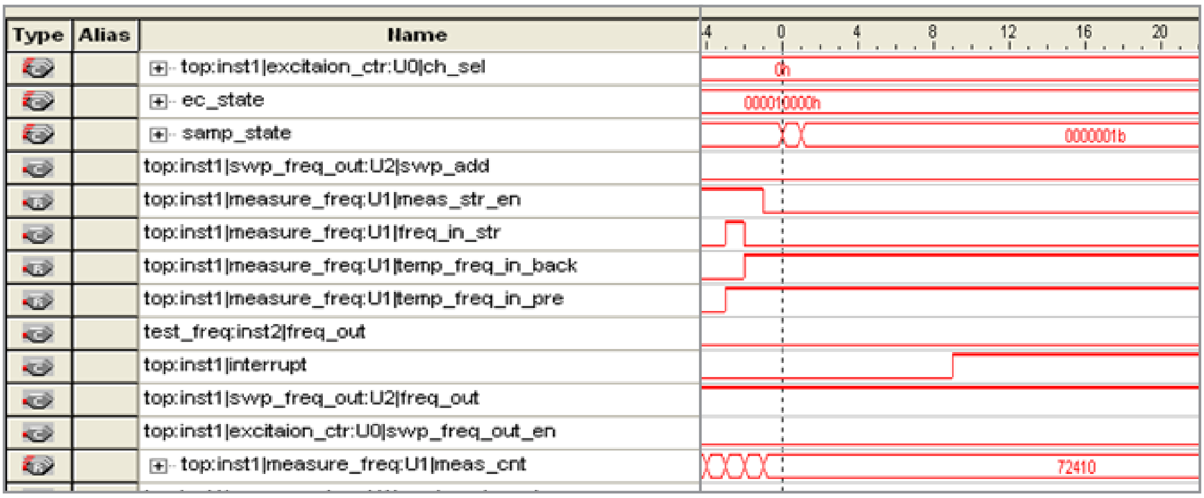

Figure 7 (meas_cnt =72410) and Interrupt Result Validation

The measurement frequency data of the current channel are stored in two registers. In dual-channel paral-lel measurement, addresses 0x10–0x11 hold the data value for one channel among channels 0–7, where-as 0x12–0x13 store the data value for one channel among channels 8–15. For single-channel mea-sure-ment, the frequency data are stored solely in the 0x10–0x11 data registers. The two data registers collec-tively form a 32-bit frequency measurement countervalue:High 16 bits: Regis-ters 0x11 (for channels 0–7) and 0x13 (for channels 8).Low 16 bits:Registers 0x10 (forchannels 0–7) and 0x12 (for channels 8–15). The 32-bit data structure is organized as shown in Table 5.

Table 5: Data structure Description

Bit	Description
0~19	Counter Value
20~27	0x0:Measurement data is correct 0x01:Measurement data error 0x02: Sweep frequency output exceeds the upper limit
28~31	Channel Number

The FPGA outputs the frequency measurement result 0xdc6a in a hexadecimal format. After the measure-ment is complete, an interrupt is assigned to the ARM processor. The ARM reads the result from the des-ignated register (e.g., 0x10–0x11 for Chan-nel 0) and transmits it via the UART interface, print-ing 0xdc6a on the serial terminal. The successful data transfer between the

FPGA and ARM confirms the communication protocol integrity, including:Interrupt handling mechanisms (e.g., GPIO or dedicated interrupt lines). Register addressing consistency for multichannel systems (channel 0 corresponds to regis-ters 0x10–0x11). The validation demonstrates the functional reliability of the hardware platform (FPGA-ARM coprocessing) and software stack (sensor data acquisition and UART transmission). The test results diagram (Figure 8) confirms stable communication between the FPGA and ARM processors [9].

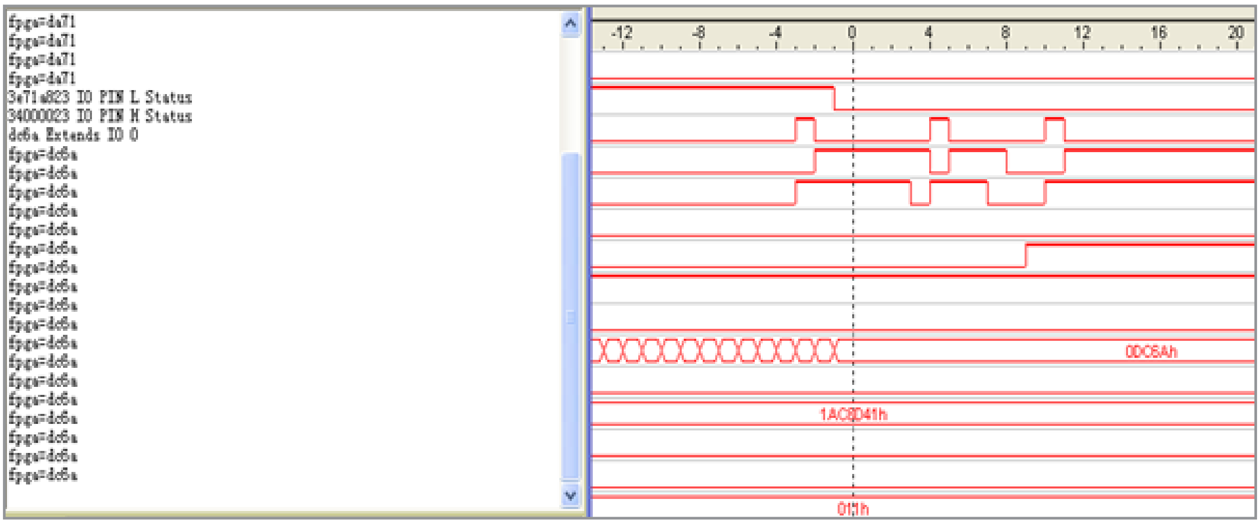

Figure 8: Test Results Diagram (FPGA=0XDC6A)

Conclusion

This study successfully developed and validated an advanced bridge stress monitoring system integrating FPGA and ARM technologies. The system effectively combines high-precision vibrating wire sensors with a robust dual-core architecture (FPGA EP4CE10E22C8N and ARM STM32F407) to achieve real-time, ac-curate stress measurements. Key features include a resonance-based excitation mechanism, a finely tuned frequency sweep and measurement system, and an efficient communication protocol between FPGA and ARM modules. The hardware platform demonstrated strong reliability, minimal error margins (as low as ±0.03%), and successful sensor data acquisition under real-world test conditions. Additionally, the modu-lar design and wireless data transmission capability position this system as a scalable and practical solu-tion for long-term bridge health monitoring and predictive maintenance. The integration of data manage-ment functions further enhances safety by providing early warning capabilities and supporting informed decision-making in infrastructure maintenance.

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