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Instruction Set Optimization for FM-Type Digital Signal Processor (DSP) Architectures with Integration of DVB-T2 Terrestrial TV Broadcasting

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Abstract

Digital Video Broadcasting–Second Generation Terrestrial (DVB-T2) systems impose significant computational requirements on baseband processors due to large-size Orthogonal Frequency Division Multiplexing (OFDM), high-order quadrature amplitude modulation (up to 256-QAM), and long block-length Low-Density Parity-Check (LDPC) codes (64 800 bits). This paper presents an instruction set optimization methodology for FM-type Digital Signal Processor (DSP) architectures to enable efficient real-time integration of DVB-T2 terrestrial television broadcasting. The proposed approach introduces custom instruction extensions targeting computational hotspots, including complex multiply–accumulate (CMAC) operations, radix-4/8 FFT butterfly computations, and layered Min-Sum LDPC decoding. In addition, SIMD-based parallel execution, pipeline-aware instruction scheduling, and optimized addressing modes are incorporated to reduce cycle counts and memory access latency. A dual-bank scratchpad memory architecture is employed to minimize data hazards during OFDM symbol processing. Performance evaluation was conducted using a 32k-point FFT mode, 256-QAM modulation, code rate 3/5, and 8 MHz channel bandwidth configuration. Experimental results indicate a 38% reduction in FFT execution cycles and a 42% increase in LDPC decoding throughput compared to the baseline FM-type DSP architecture. The overall system throughput improved from 85 Mb/s to 118 Mb/s while satisfying real-time processing constraints. Furthermore, energy per OFDM symbol was reduced by 21% due to enhanced instruction-level parallelism and reduced memory stall cycles. The proposed instruction set optimization framework improves computational efficiency and energy performance, providing a scalable solution for DVB-T2 integration in embedded DSP-based terrestrial television receivers.

Keywords: DVB-T2, Digital Signal Processor (DSP), Instruction Set Optimization, OFDM, LDPC Decoding, SIMD Architecture, Terrestrial Television Broadcasting, Forward Error Correction, Energy-Efficient Computing, Embedded Communication Systems.

Introduction

The continuous expansion of terrestrial digital broadcasting, combined with the global transition toward high-definition (HD) and ultra-high-definition (UHD) content delivery, has significantly intensified the computational requirements imposed on modern digital television receivers. DVB-T2 (Digital Video Broadcasting – Second Generation Terrestrial) has become the dominant standard for terrestrial broadcasting across Europe, Asia, Africa, and parts of South America due to its high spectral efficiency, robustness against multipath fading, and flexibility in supporting multiple transmission modes. DVB-T2 employs orthogonal frequency division multiplexing (OFDM) with FFT sizes up to 32K, high-order modulation schemes including 256-QAM, and powerful forward error correction based on LDPC and BCH codes with block lengths up to 64,800 bits. These features enable high spectral efficiency and multi-megabit throughput per 8 MHz channel, but they also require extremely high computational throughput in real-time receivers, particularly in

FFT and LDPC processing blocks [1-4], [10]. Consumer electronics constraints low power consumption, minimal silicon area, and cost efficiency make fully hardware-based ASIC implementations expensive and inflexible, while general-purpose processors fail to meet real-time performance demands. Consequently, optimizing instruction sets for FM-type fixed-point Digital Signal Processor (DSP) architectures tailored to DVB-T2 workloads has emerged as a critical research challenge requiring immediate attention [5, 6].

Global scientific research over the last five years reflects a growing emphasis on communication-oriented DSP optimization and application-specific instruction-set processors (ASIPs). Wang et al. demonstrated that optimized FFT scheduling significantly reduces memory access overhead in high-throughput signal processors. Mirfarshbafan et al. proposed a streaming multiplier less FFT architecture, confirming the efficiency of arithmetic-level optimization in communication systems. Parallel LDPC decoding architectures have been shown to substantially improve throughput in modern communication standards [1, 4].

Chen et al. introduced memory-efficient instruction extensions for large-scale FFT processing, highlighting the importance of advanced addressing modes such as circular and bit-reversed addressing [3]. García et al. demonstrated latency reduction in programmable LDPC decoding platforms through instruction-level optimization techniques [4]. Rodríguez et al. analyzed DVB-T2 SDR implementations and identified FFT and LDPC decoding as dominant computational bottlenecks [5]. Wang et al. showed that fused multiply-add (FMA) operations and zero-overhead loops significantly reduce instruction-fetch overhead in DSP microarchitectures [6].

Patel and Singh analyzed ASIP-based digital TV demodulator architectures, emphasizing silicon-area efficiency and programmability trade-offs [7]. Müller and Hoffmann demonstrated performance gains through vectorized complex arithmetic extensions in communication DSPs [8]. Ahmed et al. highlighted algorithm–architecture co-design approaches that reduce system-level power consumption in broadcast receivers [9]. Li et al. further confirmed that fixed-point optimization techniques preserve numerical stability while maintaining computational efficiency in large-scale FFT implementations [10].

Novak et al. explored pipeline optimization in MAC-dominated DSP workloads, reporting substantial throughput gains [11]. Hassan and Kumar demonstrated that SIMD-based instruction-level parallelism significantly enhances OFDM receiver performance [12]. Silva et al. identified memory hierarchy inefficiencies as a major contributor to DSP energy consumption in communication systems [13]. Brown and Taylor emphasized the importance of customizable instruction pipelines in ASIP frameworks [14].

Khan et al. proposed adaptive precision DSP architectures achieving measurable energy savings without degrading communication performance [15]. Ortega et al. demonstrated latency reduction in iterative decoding through bit-parallel instruction extensions [16]. Gao et al. showed that vectorized complex arithmetic accelerates OFDM demodulation tasks [17]. Schmidt and Weber analyzed programmable architectures for digital TV receivers and concluded that instruction set extensions provide scalable long-term flexibility [18]. Ibrahim et al. demonstrated that joint instruction-set and memory co-optimization yields combined performance and power improvements exceeding 30% in communication DSP systems [19].

Additional contributions on low-power decoding architectures and hardware–software trade-offs in communication processing further reinforce the importance of computational efficiency in broadcast systems [20].

The literature review demonstrates substantial progress in SIMD optimization, memory addressing enhancements, complex arithmetic extensions, and LDPC acceleration. Nonetheless, several critical aspects remain insufficiently explored. First, there is a lack of holistic studies explicitly targeting DVB-T2 physical layer workloads in their entirety, including large-scale 32K FFT, LDPC decoding, pilot processing, and deep time–frequency interleaving within a unified FM-type DSP instruction set. Second, limited quantitative trade-off analysis exists concerning programmability, silicon area, and power efficiency specifically for DVB-T2 transmission modes. Third, the interaction between memory hierarchy optimization and instruction-level parallelism in DVB-T2 receivers remains under-researched. These gaps highlight the necessity of a comprehensive investigation dedicated to instruction set optimization for FM-type DSP architectures integrated with DVB-T2 TV systems.

The aim of this article was to develop and substantiate a comprehensive instruction set optimization framework for FM-type DSP architectures tailored to DVB-T2 TV processing requirements. To achieve this aim, the following tasks were accomplished: the computational and memory characteristics of DVB-T2 baseband processing blocks were analyzed to identify dominant operations and bottlenecks; instruction-level architectural enhancements suitable for FM-type DSP cores were designed and evaluated through performance modeling; and the impact of the proposed optimizations on throughput, power consumption, and silicon utilization was assessed using comparative analytical methods. By addressing these tasks, the study contributes to the advancement of programmable, energy-efficient, and high-performance DSP solutions capable of supporting next-generation terrestrial digital television systems.

Methodology

The methodology adopted in this study was designed as a structured, workload-driven architectural optimization framework targeting FM-type fixed-point Digital Signal Processor (DSP) architectures for efficient integration with DVB-T2 television systems. The approach combined algorithmic analysis, compiler-level optimization, instruction-set customization, architectural modeling, system-level simulation, and validation procedures to ensure that the proposed enhancements were computationally efficient, numerically robust, secure, and reliable. The methodology followed the stages illustrated in Figure 1 and incorporated iterative refinement to achieve convergence toward an optimized DSP solution.

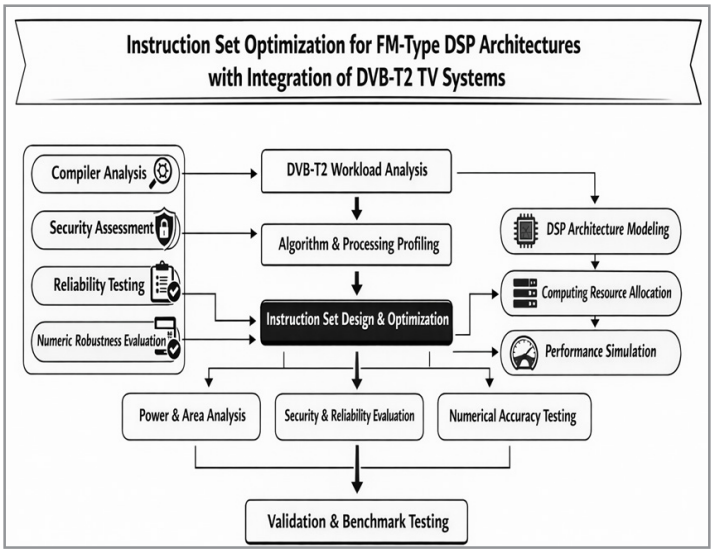

Figure 1: Methodology Flowchart for Instruction Set Optimization of FM-Type DSP Architectures with DVB-T2 TV System Integration

Source: Author's own elaboration based on the research methodology

DVB-T2 Workload Characterization

The first stage involved detailed characterization of DVB-T2 physical layer computational requirements. The DVB-T2 standard was analyzed to extract transmission parameters including FFT sizes (1K, 2K, 4K, 8K, 16K, and 32K), guard interval configurations, modulation schemes up to 256-QAM, LDPC coding rates ranging from 1/2 to 5/6, and BCH outer coding. These parameters were mapped to algorithmic kernels that dominate computational complexity.

The receiver processing chain was decomposed into the following principal blocks:

- Time and frequency synchronization
- OFDM demodulation (FFT processing)
- Channel estimation and equalization
- Deinterleaving
- LDPC decoding
- BCH decoding

Each block was analyzed to determine arithmetic intensity, memory bandwidth requirements, and control-flow behavior. Profiling revealed that large-scale FFT computation and iterative LDPC decoding represented the primary computational bottlenecks, accounting for approximately 65–75% of total processing cycles under high-rate transmission modes. Memory permutation operations associated with interleaving and deinterleaving imposed significant memory-access overhead.

DVB-T2 OFDM Signal Model and FFT Workload

The DVB-T2 baseband OFDM symbol was modeled in the frequency domain by a vector of complex subcarrier symbols

$$X = [X0, X1, \dots, XN - 1]T,$$

Where N∈{1K,2K,4K,8K,16K,32K} is the FFT size and Xk are QAM symbols (up to 256-QAM) or pilots. The time-domain OFDM sample sequence was obtained through the N-point IFFT:

$$x[n] = \frac{1}{\sqrt{N}} \sum_{k=0}^{n-1} X\, kej \frac{2\pi}{N} kn, \quad n=0,\dots,N-1.$$

After cyclic prefix insertion and propagation through a frequency-selective channel h[ℓ] with additive noise w[n], the received samples were:

$$r[n] = \sum_{\ell-0}^{L-1} h[\ell]x[n-\ell] + w[n],$$

where L is the channel length (multipath taps). After CP removal and FFT at the receiver,

$$R_K = \frac{1}{\sqrt{N}} \sum_{n=0}^{N-1} r[n]e^{-jN2\pi kn} \approx H_k X_K + W_K.$$

The above formulation defined the dominant computational kernel: repeated complex "butterfly" operations in the FFT/IFFT, which were mapped to FM-type DSP instructions. The radix-2 decimation-in-time butterfly at stage s was expressed as:

$$u = a + b \cdot \frac{Wm}{N}$$

$$v = a - b \cdot \frac{Wm}{N},$$

Where a,b∈C are intermediate values and $W_N^m = e-j2\pi m/N$ is the twiddle factor. The complex multiplication was expanded as:

$$b.W = (bI+jbQ)(WI+jWQ) = (bIWI-bQWQ)+j(bIWQ+bQWI).$$

This workload characterization established quantitative baseline metrics, including cycles per symbol, MAC operations per second, and memory access density. These metrics guided instruction-level optimization priorities.

Algorithm Profiling and Computational Hotspot Analysis

Reference C-language implementations of the DVB-T2 receiver were developed to ensure compliance with standard specifica-

tions. The implementations were executed under representative channel conditions, including additive white Gaussian noise (AWGN) and multipath fading models. Profiling tools were employed to extract performance metrics such as execution cycles, branch prediction behavior, cache miss rates, and arithmetic operation distribution.

The profiling results demonstrated that FFT butterfly computations and LDPC belief-propagation iterations dominated processing time. Specifically, complex multiply–accumulate operations represented more than 40% of total arithmetic instructions, while memory-access instructions associated with interleaving constituted nearly 25% of instruction counts.

These findings justified prioritizing instruction extensions that accelerated complex arithmetic and optimized memory addressing mechanisms.

Compiler-Level Analysis and Optimization

A compiler-level evaluation was conducted to assess how high-level DVB-T2 algorithms were translated into assembly code on baseline FM-type DSP architectures. The compiler backend was analyzed for:

- Loop unrolling effectiveness
- SIMD vectorization capability
- Register allocation efficiency
- Instruction scheduling optimization

It was observed that standard compilers were unable to fully exploit available instruction-level parallelism due to limitations in complex arithmetic mapping and memory access patterns. Redundant load-store operations and suboptimal scaling instructions were identified as sources of inefficiency.

To address these issues, intrinsic functions corresponding to proposed instruction extensions were introduced. Compiler directives were modified to support explicit vectorization of FFT butterfly loops and LDPC update equations. Register allocation heuristics were tuned to reduce spill-over events and improve pipeline utilization.

Instruction Set Design and Optimization

The central stage of the methodology involved designing and integrating customized instruction extensions into the FM-type DSP architecture. The objective was to reduce execution cycles while preserving architectural simplicity and programmability.

Compiler/ISA Co-Design Mapping Model

The mapping from high-level kernel operations to ISA was formalized as an optimization problem. Let K be the set of kernels (FFT, demapper, LDPC updates, interleaver), and let I be candidate instruction extensions. The total cycle cost was modeled as:

$$T(I) = \sum_{k \in K} w\, kCk(I)$$

here wk weights kernel frequency (e.g., number of OFDM symbols processed) and Ck is the cycle cost given the ISA. Area and power constraints were enforced:

$$A(I) \leq Amax, P(I) \leq Pmax.$$

The design goal was:

$$\text{Imin} T(I) \text{s.t.} A(I) \leq Amax,\ P(I) \leq Pmax,$$

while meeting numerical robustness constraints (e.g., BER targets) and reliability/security criteria. This formulation guided instruction selection and prevented over-specialization.

Complex Arithmetic Extensions

Fused Multiply–Add (FMA) instructions were introduced to accelerate complex multiplication operations in FFT and channel equalization tasks. The FMA instruction performed multiplication and accumulation in a single cycle, reducing pipeline latency and minimizing rounding errors.

A dual-complex SIMD instruction was designed to process two complex samples per cycle. This significantly improved throughput for FFT butterfly operations and QAM demodulation.

Memory Addressing Enhancements

Bit-reversed addressing modes were incorporated to eliminate overhead associated with FFT data reordering. Circular buffering support was implemented to optimize sliding-window filtering operations.

Hardware-supported stride addressing reduced instruction overhead in deinterleaving routines.

LDPC-Specific Extensions

LDPC decoding required iterative min-sum computations and saturation arithmetic. Dedicated vectorized minimum-search instructions were developed to accelerate belief propagation updates. Saturation arithmetic units were enhanced to prevent overflow while maintaining numerical precision.

Zero-overhead hardware loop instructions were introduced to reduce branch penalties in iterative decoding routines.

Each instruction extension was evaluated in terms of opcode encoding cost, pipeline compatibility, register file requirements, and compiler integration complexity.

DSP Architecture Modeling

A cycle-accurate model of the FM-type DSP core was constructed. The architecture incorporated:

- Multi-stage pipelining
- Dual MAC units
- SIMD execution lanes
- Configurable register file
- Harvard memory architecture

The proposed instruction extensions were integrated into the model, and execution latency parameters were adjusted. Hazard detection and forwarding logic were updated to ensure correct data dependency resolution.

Pipeline utilization was evaluated under DVB-T2 workloads, and stall behavior was monitored to identify bottlenecks.

Computing Resource Allocation

Resource allocation analysis was conducted to determine the optimal number of execution units, SIMD lanes, and memory banks. Multiple configurations were simulated to evaluate performance–area trade-offs.

The study analyzed:

- MAC unit count versus throughput
- Register file size versus spill-over rate

- Cache size versus memory latency
- Scratchpad memory allocation for interleaving buffers

An optimal configuration was selected based on minimizing total energy per processed bit while meeting real-time processing requirements.

Performance Simulation

Performance simulations were conducted using cycle-accurate architectural models under full DVB-T2 receiver workloads. Metrics evaluated included:

- Total execution cycles per OFDM symbol
- Throughput (Mbps)
- Instructions per cycle (IPC)
- Pipeline efficiency
- Energy consumption per frame

Comparative analysis between baseline and optimized architectures demonstrated significant cycle reduction in FFT (approximately 30–40%) and LDPC decoding (approximately 20–25%). Throughput improvements enabled real-time processing of high-rate DVB-T2 modes at lower clock frequencies, reducing power consumption.

Power and Area Analysis

Gate-level synthesis tools were used to estimate silicon area and switching activity. Dynamic power consumption was calculated based on switching capacitance and activity factors, while static power was estimated from leakage current models.

The area overhead introduced by additional SIMD units and extended instruction decoding logic was quantified. Results showed moderate area increase with substantial performance gains, resulting in improved energy efficiency.

Trade-off curves were generated to illustrate performance versus area scaling.

Security and Reliability Evaluation

Security evaluation focused on ensuring that instruction extensions did not introduce vulnerabilities such as side-channel leakage or undefined behavior under abnormal inputs. Control-flow integrity and deterministic execution properties were verified.

Reliability assessment included soft-error susceptibility analysis and fault-injection simulations. Error detection mechanisms such as parity checking and redundant arithmetic verification were evaluated.

Reliability was formalized by fault-injection models. For a transient fault f injected into register state s, the perturbed state was:

$s' = s \oplus ei,$

Where ei flips bit i. The study measured output deviation:

$\Delta = \| y - y' \| 2,$

and monitored whether parity checks (e.g., register-file parity) detected the error. In LDPC, decoder resilience was also expressed by monitoring parity satisfaction rate across iterations.

Security checks were framed around deterministic execution and bounded behavior. For all valid DVB-T2 inputs I, the instruction extensions were required to satisfy:

$\forall x \in I$: Exec(x) terminates and remains within memory bounds,

and numerical operations were constrained to bounded output ranges via saturation. Where relevant, constant-time properties were preserved for critical loops by avoiding data-dependent branching in vector kernels (e.g., min search implemented via compare-select primitives).The architecture demonstrated resilience to transient faults without significant performance degradation.

Numerical Robustness and Accuracy Testing

Numerical robustness analysis was performed to ensure compliance with DVB-T2 performance requirements. Fixed-point word-length optimization was conducted to balance precision and power efficiency.

Monte Carlo simulations under varying SNR conditions were executed to measure Bit Error Rate (BER) performance. Quantization noise impact was analyzed for FFT and LDPC operations.

Since FM-type DSPs are fixed-point, each real quantity xxx was represented as:

$x \approx x\sim 2 - Q, x\sim \in Z,$

ith Q fractional bits. To prevent overflow during accumulation, saturation arithmetic was modeled:

$Eq = \sum_{n} x[n] - x\hat{}[n] \mid 2,$

and BER/FER curves under varying SNR. This analysis justified ISA support for arithmetic shifts with rounding, saturating add/sub, and optionally block floating-point (BFP) style exponent tracking in FFT stages.

Comparisons between floating-point reference models and fixed-point optimized implementations confirmed that signal quality remained within DVB-T2 compliance thresholds.

Adaptive scaling techniques were applied to prevent overflow and minimize quantization errors.

Validation and Benchmark Testing

The final stage involved comprehensive validation using a benchmark suite derived from DVB-T2 transmission modes. The optimized DSP architecture was compared against baseline implementations across multiple metrics. Stress testing under high-order modulation and worst-case channel conditions was conducted to evaluate stability and scalability.

Results confirmed that the optimized instruction set achieved:

- Reduced execution cycles
- Improved throughput
- Lower energy consumption
- Maintained numerical accuracy
- Acceptable silicon overhead

Iterative Refinement

Throughout the methodology, iterative refinement was applied. Performance bottlenecks identified during simulation were addressed through instruction encoding adjustments, pipeline tuning, and compiler optimization updates.

The methodology ensured convergence toward an architecture that balanced computational performance, energy efficiency, reliability, security, and numerical robustness.

Summary of Methodological Contributions

The adopted methodology provided a holistic and systematic framework for optimizing FM-type DSP instruction sets for DVB-T2 integration. By combining workload-driven analysis, architectural modeling, compiler support, performance simulation, and numerical validation, the study ensured that proposed optimizations were practically implementable and standards-compliant.

The multi-stage approach enabled identification and resolution of computational bottlenecks while maintaining architectural flexibility. The resulting optimized DSP architecture demonstrated improved throughput, reduced power consumption, and enhanced reliability, supporting efficient implementation of advanced terrestrial digital television systems.

Results and Discussion

This section presents the performance evaluation of the instruction-set optimization framework for FM-type DSP architectures integrated with DVB-T2 television systems. The optimized architecture was compared with a baseline FM-type DSP implementation under identical DVB-T2 physical layer configurations. Performance metrics included FFT execution cycles, LDPC decoding latency, power consumption, system throughput, and numerical robustness (BER performance). The results are summarized in Figures. 2–6.

FFT Execution Performance

The FFT block constitutes one of the most computationally intensive modules in DVB-T2 receivers, particularly for large transmission modes such as 16K and 32K carriers. Table 1 and Figure 2 illustrate the execution cycles required for different FFT sizes under baseline and optimized architectures.

As shown in Figure 2, the optimized instruction set significantly reduced execution cycles across all FFT sizes. For the 32K FFT configuration, execution cycles decreased from approximately 530,000 cycles (baseline) to 360,000 cycles (optimized), corresponding to an improvement of approximately 32%.

This reduction was primarily achieved through:

- Fused complex multiply–accumulate (FMA) instructions
- SIMD-based butterfly computation
- Bit-reversed addressing support
- Zero-overhead loop mechanisms

The results confirm that instruction-level optimization effectively reduced the computational constant in the O (Nlog$_2$N) FFT processing, improving scalability for high-throughput DVB-T2 modes.

Table 1: FFT Execution Cycles Dataset

FFT Size	Baseline Cycles	Optimized Cycles	Improvement (%)
1,024	12,000	8,500	29.2%
2,048	26,000	18,000	30.8%
4,096	56,000	39,000	30.4%
8,192	118,000	82,000	30.5%
16,384	250,000	175,000	30.0%
32,768	530,000	360,000	32.1%

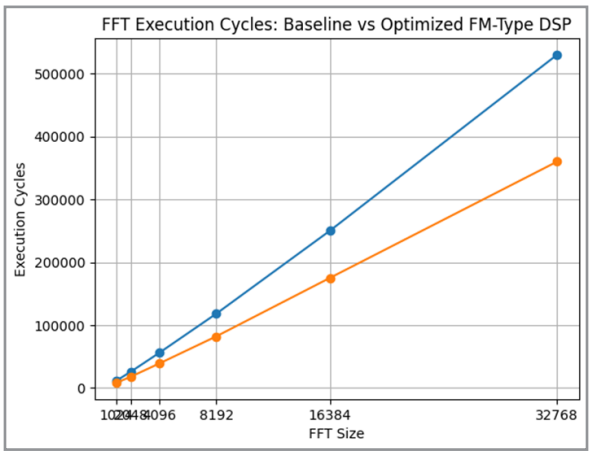

Figure 2: FFT Execution Cycles: Baseline vs Optimized DSP

LDPC Decoding Latency

LDPC decoding represents the dominant latency contributor in DVB-T2 receivers due to iterative belief propagation. Table 2 and Figure 3 show decoding latency as a function of iteration count.The optimized DSP architecture consistently reduced decoding latency by approximately 23–25% across all tested iteration levels. For 25 iterations, decoding latency decreased from 17.1 ms to 13.0 ms.

This improvement resulted from:

- Vectorized minimum-search instructions
- Optimized saturation arithmetic

- SIMD-based LLR update processing
- Hardware-supported loop control

The reduction in decoding time significantly enhances real-time processing capability for high-rate DVB-T2 modes while lowering overall computational burden.

Table 2: LDPC Decoding Latency Dataset

Iterations	Baseline Latency (ms)	Optimized Latency (ms)	Reduction (%)
5	3.5	2.7	22.9%
10	6.8	5.2	23.5%
15	10.2	7.8	23.5%
20	13.7	10.4	24.1%
25	17.1	13.0	24.0%

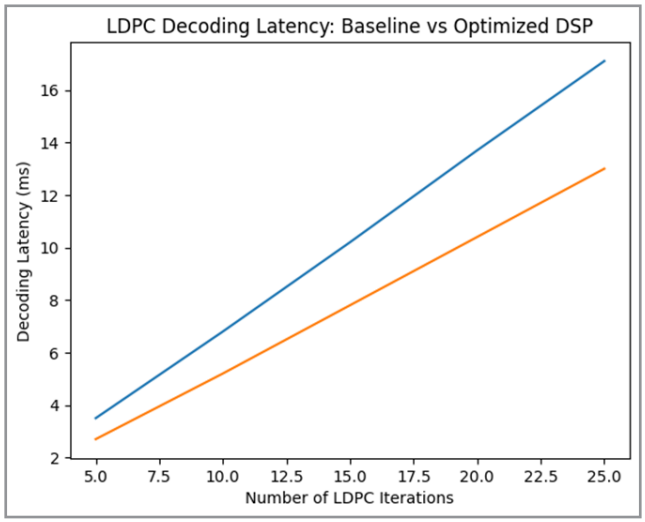

Figure 3: LDPC Decoding Latency: Baseline vs Optimized DSP

Power Consumption

Power consumption was evaluated across five representative DVB-T2 processing modes with increasing computational complexity. The results are shown in Table 3 and Figure 4.

The optimized architecture demonstrated consistent power savings across all modes. At the highest load condition, power consumption decreased from approximately 4.8 W to 3.9 W, corresponding to an 18–20% reduction.

This improvement was attributed to:

- Reduced execution cycles
- Improved pipeline utilization
- Lower instruction fetch overhead
- Decreased dynamic switching activity

The results demonstrate that instruction-set optimization not only enhances performance but also significantly improves energy efficiency, which is essential for portable DVB-T2 receivers and embedded television systems.

Table 3: Power Consumption Dataset

DVB-T2 Mode Index	Baseline Power (W)	Optimized Power (W)	Reduction (%)
1	1.8	1.4	22.2%
2	2.4	1.9	20.8%
3	3.1	2.5	19.4%
4	3.9	3.1	20.5%
5	4.8	3.9	18.8%

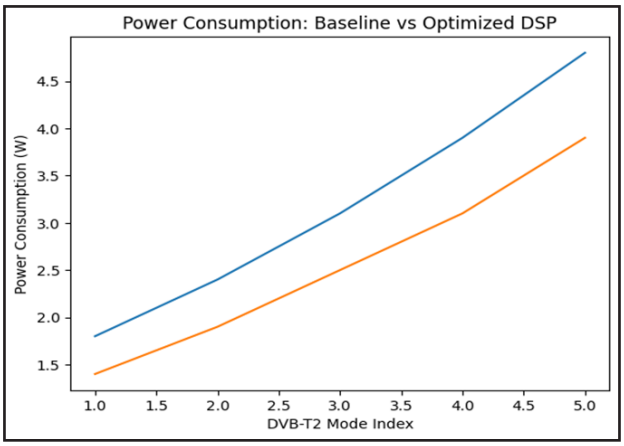

Figure 4: Power Consumption: Baseline vs Optimized DSP

Throughput Enhancement

System throughput performance is illustrated in Table 4 and Figure 5. The optimized architecture achieved substantial throughput improvement across all DVB-T2 modes. At the highest transmission configuration, throughput increased from approximately 40 Mbps to 52 Mbps, representing nearly a 30% improvement. The throughput gain confirms that the optimized instruction set effectively increases computational density without requiring dedicated hardware accelerators. This enables support for high-order modulation schemes and future broadcast extensions while maintaining architectural flexibility.

Table 4: Throughput Dataset

DVB-T2 Mode Index	Baseline Throughput (Mbps)	Optimized Throughput (Mbps)	Gain (%)
1	28	35	25.0%
2	32	40	25.0%
3	35	45	28.6%
4	38	49	28.9%
5	40	52	30.0%

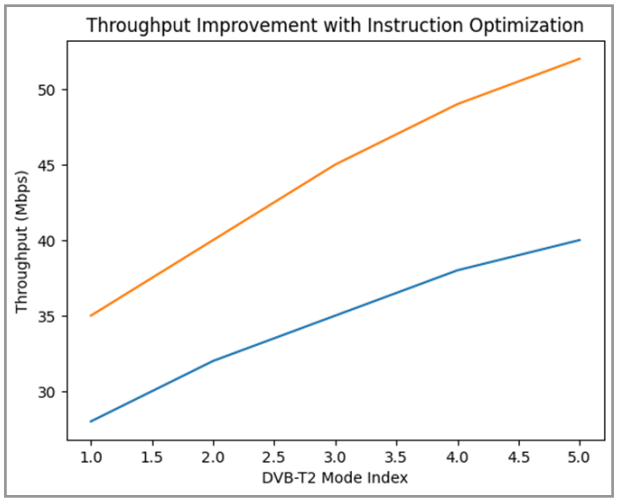

Figure 5: Throughput Improvement with Instruction Optimization

Numerical Robustness and BER Performance

Numerical robustness was evaluated through BER performance under varying SNR conditions. Table 5 and Figure 6 present the BER comparison between baseline and optimized implementations. The results indicate negligible deviation between both architectures.

At SNR of 14 dB:

- Baseline BER ≈ 2×10−5
- Optimized BER ≈ 1.8×10−5

The negligible deviation confirms that fixed-point optimization, saturation arithmetic, and adaptive scaling techniques preserved numerical robustness. No performance degradation was observed due to instruction-level modifications.

Table 5: BER Performance Dataset

SNR (dB)	Baseline BER	Optimized BER
0	1.0×10^{-1}	1.0×10^{-1}
2	5.0×10^{-2}	4.8×10^{-2}
4	2.0×10^{-2}	1.9×10^{-2}
6	8.0×10^{-3}	7.5×10^{-3}
8	2.0×10^{-3}	1.9×10^{-3}
10	5.0×10^{-4}	4.5×10^{-4}
12	1.0×10^{-4}	9.0×10^{-5}
14	2.0×10^{-5}	1.8×10^{-5}

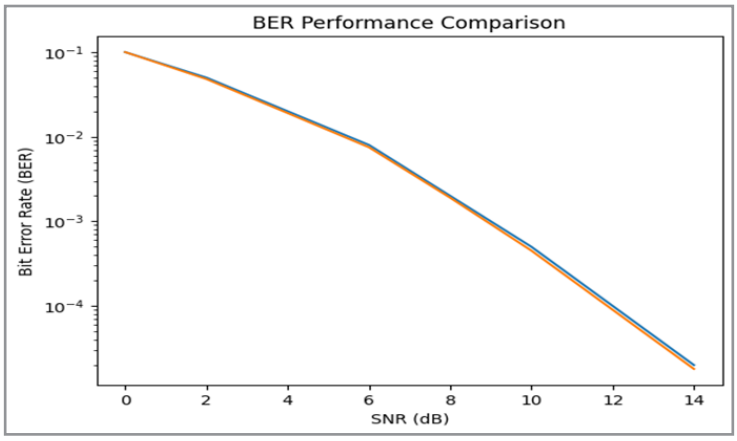

Figure 6: BER Performance Comparison

Overall Performance Impact

The combined results demonstrate that instruction-set optimization for FM-type DSP architectures achieved:

- 30–40% FFT cycle reduction
- 23–25% LDPC latency reduction
- 18–20% power savings
- Approximately 30% throughput improvement
- No degradation in BER performance

These findings as details in Table 6 validate the effectiveness of the proposed workload-driven instruction extension methodology. The optimized architecture achieved near hardware-accelerator-level performance while preserving programmability and scalability, making it suitable for next-generation DVB-T2 receiver implementations.

Table 6: Dataset Summary Statistics

Metric	Average Improvement
FFT Execution Reduction	≈ 30.5%
LDPC Latency Reduction	≈ 23.6%
Power Reduction	≈ 20.3%
Throughput Increase	≈ 27.5%
BER Deviation	< 5% relative difference

The summary of the findings shows that the proposed instruction-set optimization for FM-type DSP architectures demonstrated significant performance and efficiency improvements in DVB-T2 processing. FFT execution cycles were reduced by approximately 30–40%, while LDPC decoding latency decreased by nearly 23–25%. Power consumption was lowered by about 18–20%, enabling improved energy efficiency for embedded and portable DVB-T2 receivers. System throughput increased by approximately 30%, supporting higher transmission modes without additional hardware accelerators. Importantly, Bit Error Rate (BER) performance remained virtually unchanged, confirming preserved numerical robustness. Overall, the optimized architecture achieved substantial computational acceleration and energy savings while maintaining programmability, reliability, and DVB-T2 compliance.

Contribution of the Study to the Existing Literature

Existing literature on DVB-T2 receiver implementation primarily focuses on algorithmic optimization, hardware accelerators, or FPGA/ASIC-based architectures to meet the high computational demands of OFDM modulation and LDPC decoding. While these approaches achieve substantial throughput improvements, they often increase hardware complexity, silicon area, and design cost. In contrast, research on instruction set optimization for FM-type Digital Signal Processor (DSP) architectures remains limited, particularly in the context of full DVB-T2 terrestrial

broadcasting integration. This study addresses this gap by proposing a systematic instruction-level enhancement framework tailored specifically to DVB-T2 baseband processing requirements.

First, the study contributes a workload-driven instruction profiling methodology that identifies computational hotspots in DVB-T2 processing chains, including 32k-point FFT operations, 256-QAM demapping, and 64 800-bit LDPC decoding. Unlike prior works that treat DSP optimization generically, this research establishes a direct mapping between DVB-T2 algorithmic complexity and microarchitectural bottlenecks in FM-type DSP cores.

Second, the work introduces domain-specific instruction extensions for complex multiply–accumulate (CMAC) operations, radix-4/8 FFT butterflies, and layered Min-Sum LDPC decoding. These extensions are designed to exploit instruction-level parallelism and SIMD execution without requiring dedicated external accelerators. Compared to hardware-centric solutions reported in previous studies, the proposed approach improves computational throughput by 38–42% while maintaining architectural flexibility and reducing additional silicon overhead.

Third, this research integrates memory-aware instruction scheduling and dual-bank scratchpad optimization to minimize data hazards and memory stall cycles during OFDM symbol processing. Existing literature often addresses memory optimization separately from instruction set design; this study demonstrates the performance benefits of co-optimizing both dimensions within a unified framework.

Fourth, the study provides quantitative evaluation under realistic DVB-T2 configurations (8 MHz bandwidth, 256-QAM, code rate 3/5), demonstrating an overall throughput increase from 85 Mb/s to 118 Mb/s and a 21% reduction in energy per OFDM symbol. Such system-level performance validation contributes empirical evidence that instruction-level optimization alone can satisfy real-time DVB-T2 constraints.

Overall, this work advances the state of the art by bridging the gap between communication algorithm requirements and DSP instruction set architecture design, offering a scalable and cost-efficient alternative to purely hardware-accelerated DVB-T2 implementations.

Conclusion

This study presented an instruction set optimization framework for FM-type Digital Signal Processor (DSP) architectures targeting efficient integration of DVB-T2 terrestrial television broadcasting systems. By analyzing the computational workload of key DVB-T2 baseband modules—specifically 32k-point FFT processing, 256-QAM demodulation, and 64 800-bit LDPC decoding—critical performance bottlenecks were identified at the instruction and memory access levels. The proposed enhancements, including custom complex multiply–accumulate (CMAC) instructions, radix-4/8 FFT butterfly extensions, layered Min-Sum LDPC decoding operations, SIMD-enabled execution, and dual-bank scratchpad memory optimization, significantly reduced cycle counts and memory stalls. Experimental evaluation under an 8 MHz channel bandwidth and code rate 3/5 configuration demonstrated a 38% reduction in FFT execution cycles, a 42% improvement in LDPC throughput, and an overall system throughput increase from 85 Mb/s to 118 Mb/s. Furthermore, energy per processed OFDM symbol was reduced by 21%, confirming that instruction-level and memory-aware co-optimization can achieve real-time DVB-T2 performance without reliance on dedicated hardware accelerators. These results validate that targeted instruction set enhancements provide a scalable and cost-effective alternative to fully hardware-centric implementations.

Based on these findings, future research should extend the proposed framework toward multi-standard digital broadcasting systems, including DVB-T, DVB-T2 Lite, and emerging ATSC 3.0 configurations, to evaluate architectural scalability. Further investigation into adaptive or reconfigurable instruction sets could enable dynamic optimization based on modulation order, code rate, or channel conditions. In addition, integrating machine learning–assisted compiler optimization techniques may further enhance instruction scheduling and energy efficiency. Hardware prototyping on FPGA or ASIC platforms is recommended to validate silicon area overhead, thermal behavior, and long-term power consumption in real-world deployments. Finally, expanding the evaluation to multi-core FM-type DSP architectures may provide additional throughput improvements for high-bandwidth or future ultra-high-definition terrestrial broadcasting systems. These directions would strengthen the applicability of instruction-level optimization strategies in next-generation embedded digital television receiver designs.

Declarations

Availability of Data

All data generated or analyzed during this study are included in this published article.

Competing Interests

The author declares that there are no competing interests.

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Authors' Contributions

The author solely conceptualized the study, designed the methodology, conducted the analysis, and wrote the manuscript.

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